WHAT IS CLAIMED IS:

1. A method of testing a chip that comprises an intellectual product circuit module, the method comprising:

providing a test pattern;

configuring a plurality of registers in a plurality of different states according to the test pattern; and

providing a test activating signal to the intellectual product circuit module in a next state, so that the intellectual product circuit module operates according to the test pattern.

2. A circuit for testing a chip that comprises an intellectual product circuit module, the circuit comprising:

a plurality of registers, coupled to the intellectual product circuit module to output signals stored in the registers to the intellectual product circuit module; and

a mutiplexing finite state machine controller, coupled to the intellectual product circuit module and the registers, wherein

the mutiplexing finite state machine controller receives a test pattern and configures the registers in a plurality of different states, in the next state the mutiplexing finite state machine controller further provides the test activating signal to the intellectual product circuit module so that the intellectual product circuit module is operated and tested according to outputs of the registers.

3. The circuit according to claim 2, wherein the intellectual product circuit module further comprises a plurality of ports coupled to the registers.

4. The circuit according to claim 2, wherein the test activating signal includes a synchronous clock signal.

5. The circuit according to claim 2, wherein each of the registers further comprises

an enable input terminal coupled to the mutiplexing finite state controller capable of controlling the registers and asserting an enable signal to enable the registers to buffer the test pattern.

6. A circuit for testing a chip that comprises a plurality of intellectual product circuit modules, the circuit comprising:

a multiplexer controller, coupled to the intellectual product circuit modules to selectively output a test result from the intellectual product circuit modules;

a plurality of registers, coupled to the intellectual product circuit modules to output signals stored in the registers to the intellectual product circuit modules; and

a mutiplexing finite state machine controller, coupled to the intellectual product circuit modules, the multiplexer controller and the registers, the mutiplexing finite state machine controller receiving a test pattern to configure the registers in a plurality of different states, and providing a test activating signal to one of the intellectual product circuit modules in a next state, so that the intellectual product circuit module is operated according to the output of the registers, and the mutiplexing finite state machine controller further controlling the multiplexer controller to selectively output the test results.

7. The circuit according to claim 6, wherein each of the intellectual product circuit modules comprises a plurality of ports coupled to the registers.

8. The circuit according to claim 6, wherein the multiplexer controller further comprises a select input terminal coupled to the mutiplexing finite state machine controller, so that the mutiplexing finite state machine controller controls the multiplexer controller to selectively output the test result.

9. The circuit according to claim 6, wherein the test activating signal comprises a synchronous clock signal.

10. The circuit according to claim 6, wherein each of the registers further comprises an enable input terminal coupled to the mutiplexing finite state machine controller, which respectively controls and enables the registers to buffer the test pattern.

11. The circuit according to claim 6, wherein the chip is a system on chip.